B. Sc. III Semester (Electronics) - (2013-14)

Digital Electronics-II) BE-301

MODEL ANSWER (AS-2791)

Section-[A]

i. (B) ii. (A) iii. (D) iv. (C)

v. (C) vi. (C) vii. (D) viii. (B)

Ans-(ix):

In JK flip flop when the value of J and K =1 and at the same time value of clock is 1, so according to the truth table of J = K =1 the value of output should be toggled so the value keep on changing till the change in the clock pulse is known as Race around condition.

Ans-(x):

$f_c = 1/\Delta t, = 1/10^{-7} = 10^7 Hz.$

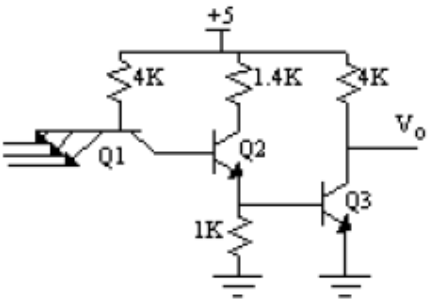
Section-[B]

Ans-2:

Transistor–transistor logic (TTL) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called transistor–transistor logic because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors. TTL is notable for being an integrated circuit (IC) family used in many applications such as computers, industrial controls, test equipment and instrumentation etc.

Verification of NAND Gate:

The evolution from DTL to TTL can be seen by observing the placement of p-n junctions.
For example, the diode in DTL can be replaced by a transistor whose collector is pulled up to the power supply. The p-n junction of D2 is replaced by the BE junction of Q2 and with the current gain of the transistor, the current going into the base of Q3 is greatly increased, increasing the fanout.

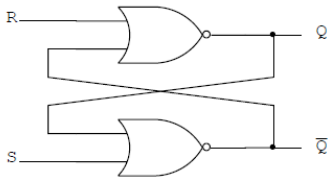


Truth Table of NAND Gate:

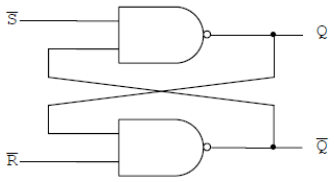
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Ans. 3:

A flip-flop is a memory device that samples and acts upon its input lines only when it is told to do so with a special timing signal called the clock. This may be in the form of a level or an edge. A level trigger means that the flip-flop samples its inputs depending upon the voltage level of the trigger input. An edge trigger means that the flip-flop samples its inputs depending on a LOW-to-HIGH transition on the trigger line or a HIGH-to-LOW transition on a trigger line.



Cross-coupled NOR RS latch

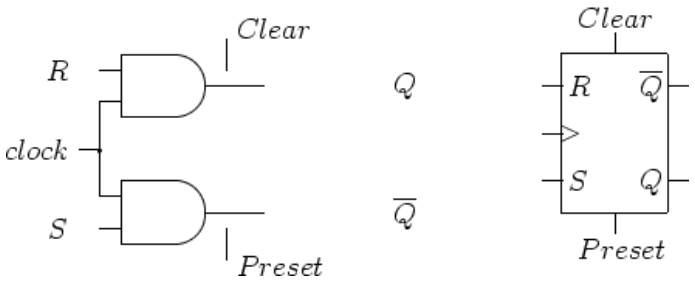


Cross-coupled NAND RS latch

The latch is a logic block that has 2 stable states (0) or (1). The RS latch can be forced to hold a 1 when the Set line is asserted. The RS latch can be forced to hold a 0 when the Reset line is asserted. The RS latch will hold it current value (state) if the Set and Reset lines are not asserted. The circuit for he RS latch can be seen below.

Truth Table

Inputs			Output Q	Operation performed
CK	Cr	Pr		
1	1	1	Q_{n+1}	Normal Flip-flop
0	0	1	0	Clear
0	1	0	1	Present



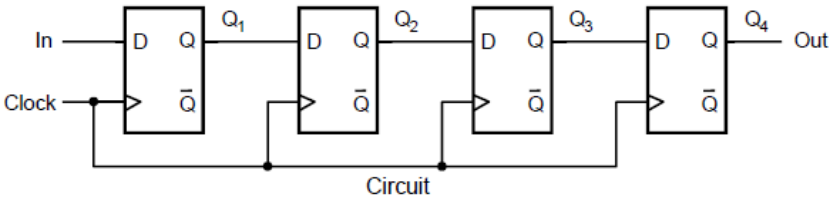
The inputs are called preset and clear. They affect the flip-flop without the need for a clock pulse. These inputs can be useful to bring the flip-flop to an initial state prior to its clocked operation. In practice, it is often preferable to clear the flip-flops on the active edge of the clock. Set S to 0 and R to 1. This resets the flip-flop which means that Q is a 0 and Q' is a 1. This will always be the case when S=0 and R=1 regardless of the previous state of Q. Go from S=0 and R=1 to S=0 and R=0. Q stays at 0 because SR=00 is the no change input combination and the previous state of Q was a 0. Set S to 1 and R to 0. This input combination sets the flip-flop (Q=1, Qi=0) regardless of the previous state of Q. Go from SR=10 to SR=00. This time Q stays at 1 which confirms that Q does not change state if S and R are 00. Set S to a 1 and R to a 1. This input combination is disallowed since Q and Q' are both 0 and are not complements of each other.

Ans.-4:

A register is a memory device that can be used to store more than one bit of information. A register is usually realized as several flip-flops with common control signals that control the movement of data to and from the register. A shift register is a register whose data can be shifted right or left. A register which is capable of shifting its binary information either to the right or to the left is called a shift register. It consists of a number of flip-flops cascaded together with the output of one flip-flop connected to the input of the next. All flip-flops in the register receive a common clock pulse that causes the shift from one state to the next.

A shift register is useful since a given binary number is multiplied by 2 if its bits are shifted one bit position to the left. Similarly, a number is divided by 2, if the bits are shifted one position to the right.

A simple shift register.



A sample sequence

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

Ans-5:

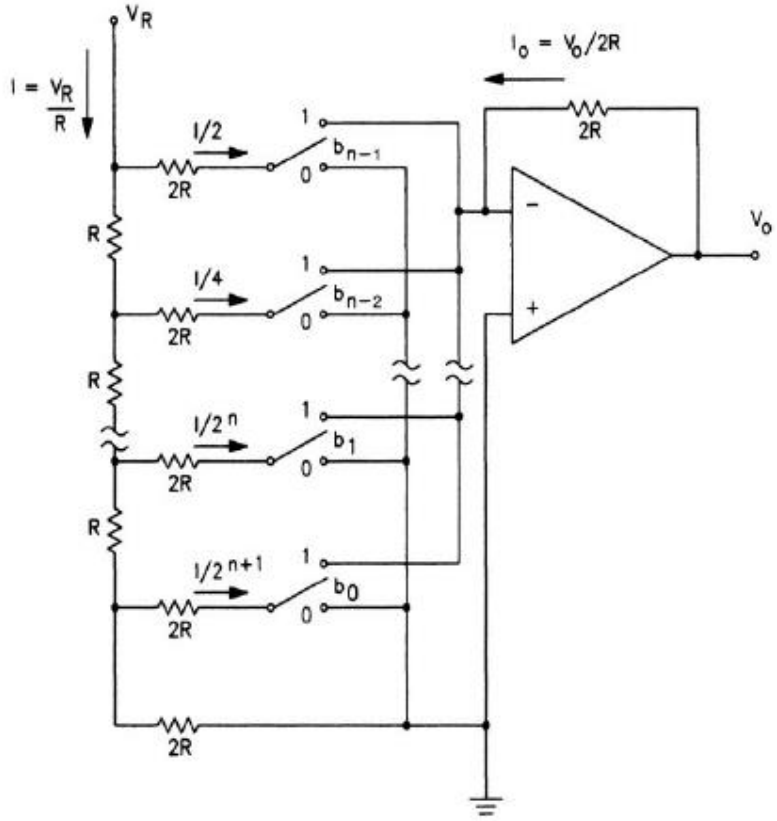
Analog refers to physical quantities that vary continuously instead of discretely. Physical phenomena typically involve analog signals. Examples include temperature, speed, position, pressure, voltage, altitude, etc. For a digital system to interact with analog systems, conversion between analog and digital values is needed. Building blocks to perform the conversions are: (1) Digital to analog converters (DAC), (2) Analog to digital converters (ADC).

A digital to analog converter has a digital input that specifies an output whose value changes in steps. These step changes are in volts or amperes. The analog to digital converter has an input that can vary from a minimum to a maximum value of volts or amperes. The output is a digital number that represents the input value.

Analog number = (bn-1 2–1 + bn-2 2–2 + … +b0 2–n) x stepsize + offset

= (digital number x step size) + offset

Digital number = (analog number – offset)/ (step size)



A DAC takes an n- bit digital input and output a corresponding analog voltage. DAC systems normally consist of three components: (a) A reference voltage, (b) The DAC itself, (c) An op amp for output buffering. Many digital-to-analog converters use R-2R ladder network. The switches are analog switches controlled by digital signals. The output voltage (Vo) is proportional to the binary input. Each branch of the ladder network contributes current whose value is proportional to the bit weight of that branch. The amplifier circuit sums the current components to produce a voltage proportional to the binary input.

Ans.6:

(a) Edge triggering is when the flip-flop state is changed as the rising or falling edge of a clock signal passes through a threshold voltage. An edge-triggered flip-flop that changes states at the positive edge (rising edge) of the clock pulse on the control input is known positive edge triggered and when it changed the state at the negative edge (falling edge) of the clock pulse on the control input is known as negative edge triggered.

(b) Find out the Analog equivalent voltage of binary 1110 if the reference voltage is 2.2V?

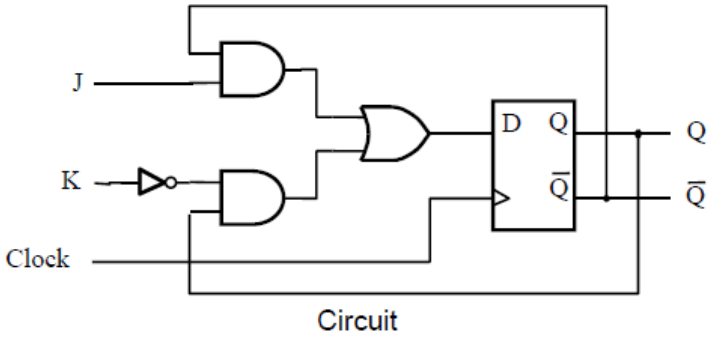
Ans: Given VR=2.2 V and n=4

We know that analog voltage $V = \frac{V_R}{2^n-1}[2^{n-1}a_{n-1} + 2^{n-2}a_{n-2} + \cdots \ldots . 2^1a_1 + 2^0a_0]$

=2.2/15[8x1+4x1+2x1+1x0]= 2.05 Volt

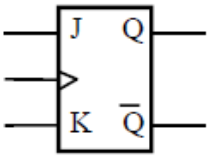
Ans.7:

CLOCK	J	K	$\overline{SET}$	$\overline{RESET}$	Q	$\overline{Q}$
-	-	-	0	1	1	0
-	-	-	1	0	0	1
↓	0	0	1	1	Q	$\overline{Q}$
↓	1	0	1	1	1	0
↓	0	1	1	1	0	1
↓	1	1	1	1	$\overline{Q}$	Q



Circuit

J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)



The JK is a refinement of the SR flip-flop in that the indeterminate state Flip-Flops, Registers, and Counters of the SR is defined in the JK type. To differentiate between the standard SR and this new variant (without an indeterminate state), the Sand R inputs are simply renamed in the JK flip-flop: J = Set (S); and K = Reset (R).

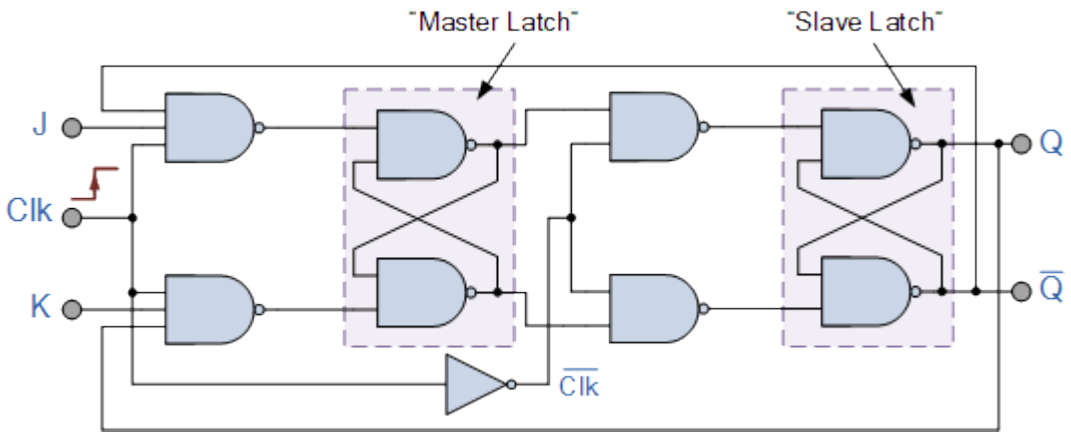
In the JK flip-flop, if both the J and K inputs are 1, both cannot pass the signal and there is race around condition. If Q=1 the K signal can pass through and, upon application of the clock pulse, the flip-flop is cleared. When Q'=1, the J signal can pass through and, upon application of the clock pulse, the flip-flop is set. In either case, for J=K=1, the output of the flip-flop is complemented.

In the initial condition when all the inputs are zero i.e. J=0 and K=0 the output remains unchanged as there is no any active reaction in the J-K flip flop.

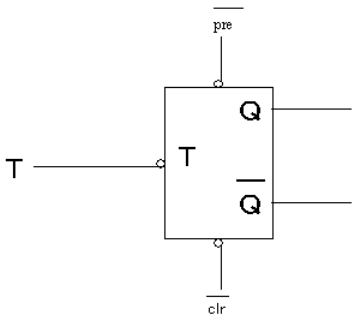
Ans.-8:

The Master-Slave Flip-Flop is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip-flop being connected to the two inputs of the "Slave" flip-flop. This feedback configuration from the slave's output to the master's input gives the characteristic toggle of the JK flip-flop as shown below.

J	K	Clk	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0



T-Type Flip-flop:

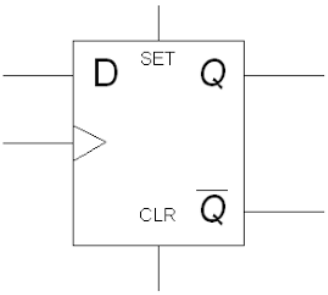


Truth Table:

Input T_n	Output Q_{n+1}
0	Q_n
1	Q_n'

The T type flip-flop is a single input device T (trigger). Two outputs: Q and Q' (where Q' is the inverse of Q). The operation of the T type flip-flop is as follows: A '0' input to 'T' will make the next state the same as the present state (i.e. T = 0 present state = 0 therefore next state = 0). However a '1' input to 'T' will change the next state to the inverse of the present state (i.e. T = 1 present state = 0 therefore next state = 1). The T type flip-flop is an edge driven device. Therefore you should not associate 1 and 0 with levels, but instead 1 should be considered as a pulse, and 0 as no pulse.

D type flip-flop (Delay)



Truth Table:

Input D_n	Output Q_{n+1}
0	0
1	1

The D type flip-flop has one data input 'D' and a clock input. The circuit edge triggers on the clock input. The flip-flop also has two outputs Q and Q' (where Q' is the reverse of Q). Any input appearing (present state) at the input D, will be produced at the output Q in time T+1 (next state). e.g. if in the present state we have D = 0 and Q = 1, the next state will be D = anything and Q = 0. When T=1 and CP=1, the flip-flop complements its output, regardless of the present state of the Flip-flop. In this case the next state is the complement of the present state. When T=0, there is no change in the state of the flip-flop (i.e.) the next state is same as the present state of the flip-flop. From the characteristic table and characteristic equation it is quite evident that when T=0, the next sate is same as the present state.